



Yield and Variability Optimization of Integrated Circuits

Jian Cheng Zhang, M.A. Styblinski

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Traditionally, Computer Aided Design (CAD) tools have been used to create the nominal design of an integrated circuit (IC), such that the circuit nominal response meets the desired performance specifications. In reality, however, due to the disturbances of the IC manufacturing process, the actual performances of the mass produced chips are different than those for the nominal design. Even if the manufacturing process were tightly controlled, so that there were little variations across the chips manufactured, the environmental changes (e. g. those of temperature, supply voltages, etc.) would also make the circuit performances vary during the circuit life span. Process-related performance variations may lead to low manufacturing yield, and unacceptable product quality. For these reasons, statistical circuit design techniques are required to design the circuit parameters, taking the statistical process variations into account. This book deals with some theoretical and practical aspects of IC statistical design, and emphasizes how they differ from those for discrete circuits. It describes a spectrum of different statistical design problems, such as parametric yield optimization, generalized on-target design, variability minimization, performance tuning, and worst-case design. The main emphasis of the presentation is placed on the principles and practical solutions for performance variability minimization. It is hoped that the book may serve as an introductory reference material for various groups of IC designers, and the methodologies described will help them enhance the circuit quality and manufacturability. The book contains seven chapters.

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